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Optimization of MBE-grown GaAs planar doped barrier diode structures

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The planar doped barrier (PDB) GaAs structures are used in many high-speed semiconductor devices [1] including microwave planar doped barrier diodes (PDBDs). These unipolar diodes have a multi layer semiconductor structure (Fig. 1) with ultra thin p^{++} layer sandwiched between two undoped layers. That structures can be synthesized only using modern epitaxial technologies, i.e. MBE or MOCVD. The current conduction mechanism in PDBD is governed by the thermionic emission of the major carriers over the built-in potential barrier. Since the barrier is formed in the bulk of the structure, better stability and lower noise are expected comparing to the Schottky diodes having surface-barrier. The further advantage of the PDBDs is the adjustable height of the barrier. This fact allows to fabricate low-barrier microwave diodes for zero-bias detectors and low-drive mixers [2].

The key point for fabrication of reproducible PDB structures is p^{++} layer charge and position control [3]. Another main factor is the low level of background doping. Therefore MBE seems to be the most suitable technology for these devices. There are two types of PDB structures: one of them is on the high-conductivity n^+ substrates and another one is on the semi-insulating substrates. The first type provides more simple diode technology but the second type is needed for realization of planar and coplanar diode constructions. These diode constructions are appropriated for MIC and millimeter wave devices [4].

There are some specific problems in MBE growth of PDBD structure on SI substrate. This structure must have two relatively thick n^+ layers. The thick bottom layer is used to provide low series resistance. It usually has thickness of 4–5 μm . The top n^+ layer is used for alloy ohmic contact formation. Reduction in thickness of the top n^+ layer beyond 0.3 μm would lead to practical problems in alloy ohmic contact fabrication. Usually the MBE growth is carried out at 600°C at growth rate of 1 $\mu\text{m}/\text{h}$. Consequently the long MBE process is typical for PDBD structure on the SI substrate.

In this work we present new design and technology for planar PDBDs. The main features of our approach are as follows:

1. Combination of vapor phase epitaxy with MBE. VPE is used for growth of thick bottom n^+ layer. The other layers were grown by MBE.
2. n^+ $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}/\text{grad InGaAs/GaAs}$ contact layer and non-alloyed Ti/Pt/Au top ohmic contact were used instead of the standard n^+ GaAs/AuGe/Ni/Au alloy contact. This approach provides the low contact resistance ($< 6 \times 10^{-6} \Omega \text{ cm}^2$) and high yield ($> 90\%$).

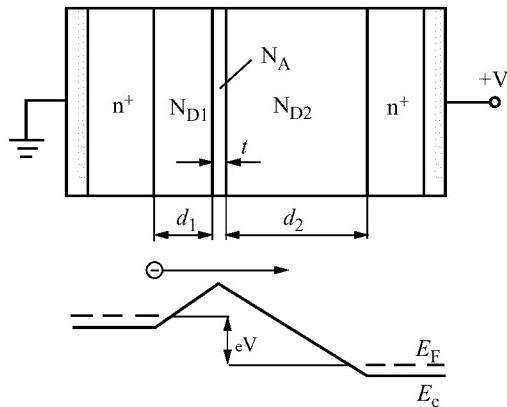


Fig 1. The structure and band diagram of the PDBD. ($t < 100 \text{ \AA}$, $N_A < 10^{18} \text{ cm}^{-3}$, $d_1 < 100 \text{ \AA}$, $d_2 < 5000 \text{ \AA}$).

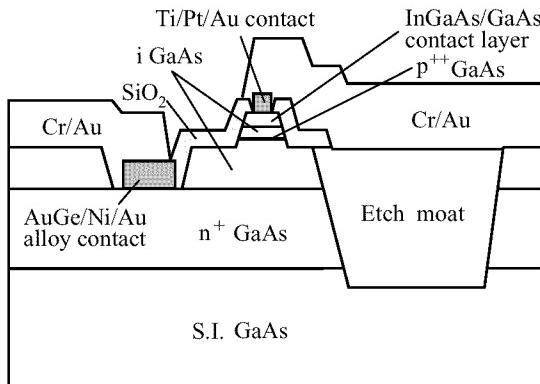


Fig 2. Designed PDBD structure.

3. For millimeter wave frequency applications planar diodes are required [4]. For this reason an existing process for the planar mixer GaAs Schottky diode manufacturing was adopted for the PDB structures. The designed PDBD structure is shown in Fig. 2.

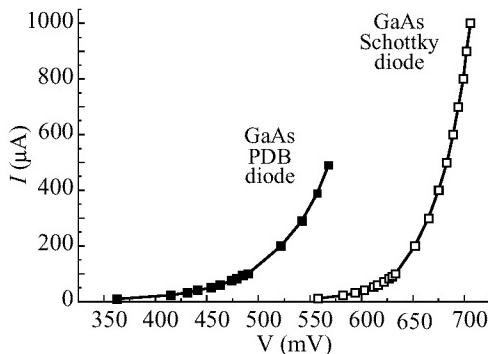
Process-development wafers were grown by MBE in Ioffe Physico-Technical Institute on Si-doped n^+ GaAs (100) substrates. Before growing the films the substrates were thermally outgassed in the growth chamber at 610°C for 10 minutes under As₄ flux. The MBE growth was carried out at 600°C at growth rate of 1 $\mu\text{m}/\text{h}$ under As stabilized condition. Si and Be were used as n - and p -dopants, respectively.

The device construction and technology were performed in the Svetlana-Electronpri-bor. Device numerical modelling and characterization were made in State Electrotechnical University. Test structures were fabricated to evaluate the PDB structure parameters. They consisted of chips with 70 μm diameter etched mesas and AuGe-Ni-Au top and bottom metallizations. DC performance of some test devices are summarized in Table 1 (where Φ_b is potential barrier height, n is ideality factor).

Then semiconductor structure parameters were extracted from I-V and C-V measurements using inverse modelling approach. The simple PDBD model [1] were used

Table 1. Test PDBDs parameters.

β	Sample	α							
		d_1 nm	d_2 nm	t nm	N_A cm^{-3}	n_{calc}	n_{exp}	Φ_{bcalc} mV	Φ_{bexp} mV
2	2-640	200	100	10	$4 \cdot 10^{17}$	1.5	1.52	368	577
3	2-680	150	30	10	10^{18}	2.2	1.34	344	476

**Fig 3.** Mesured currrent-voltage characteristics.

for this purpose in combination with numerical modelling of C–V characteristics [5].

The PDB structure and growth process parameters were optimized using obtained experimental results. The n^+ -GaAs/SI-GaAs epitaxial structure was fabricated by VPE in JSC Elma-Malachite (Moscow, Russia). Then GaAs PDB structure with InGaAs/GaAs contact layer was grown by MBE in PTI and planar diodes were fabricated. Typical room temperature forward bias I–V characteristics for PDBD and GaAs Schottky diodes are shown in Fig. 3. Comparison is made with a standard planar microwave GaAs Schottky diode with same contact configuration. It can be seen that the PDB diode has lower barrier height.

An initial assessment has shown that the low frequency noise generation ($IF < 1$ MHz) is significantly less for the PDB diodes then for GaAs Schottky diodes. Microwave measurements were made in a balanced mixer over the frequency range of 9–10 GHz.

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